Phone: Off: +91-40-23152216
Web : www.jntuh.ac.in
E Mail: manzoorjntu@gmail.com

ACCREDITED BY NAAC
A-GRADE

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

(Established by Govt. Act No. 30 of 2008)

Kukatpally, Hyderabad – 500 085, Telangana, India.

Circular No. JNTUH/DAP/A3/1510/2022 Date. 20.07.2022

Sub: JNTUH-Directorate of Academic & Planning – To offer Industry Ready Professional Training in VLSI Design/Embedded System Design course to B.Tech. ECE/EEE/EIE/CSE IV Year I & II Semesters.

Ref: 1. Proposal dated. 23.06.2022 of the Director, VEDA IIT, Hyderabad.
2. Committee members met on 11.07.2022 & 12.07.2022.
3. Note orders of the Vice-Chancellor dated. 16.07.2022.

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Vide reference (3) cited above, based on the recommendations of Head of the Departments & BoS Chairpersons, the Hon'ble Vice-Chancellor is pleased to accord permission to offer 'Industry Ready Professional Training' course in VLSI Design/ Embedded System Design to B. Tech. - ECE/EEE/EIE/CSE IV Year I & II Semester. The students of B. Tech. - ECE/EEE/EIE/CSE IV Year I & II Semester can opt for the courses offered by VEDA IIT, Hyderabad in collaboration with Consortium of Industries viz., M/s. SoCtronics Technologies Private Limited, M/s. INVECAS Technologies Private Limited & M/s. ATAI Labs Private Limited, Hyderabad. The courses offered by JNTUH for Constituent & Affiliated Colleges in IV B. Tech. I & II Semesters for 40 (20+20) credits can be suitably modified with the courses offered by VEDA IIT, Hyderabad for 40 credits to make the students industry ready in the area of VLSI Design or Embedded System Design for B. Tech. - ECE/EEE/EIE/CSE IV Year I & II Semester students.

The details are as follows:

1. These 2 semester courses are being sponsored by the consortium of industries in collaboration with VEDA IIT to improve job opportunities in VLSI/ Embedded System Design as there is substantial demand for the skilled undergraduates in these areas.
2. Selection of students for the above is based on merit test conducted by JNTUH & VEDA IIT before the commencement of IV Year B.Tech. Shortlisted students will be called for interview and the selected candidates will be offered to undergo IV year I & II semester course classes/training at VEDA IIT.
3. The credits earned by the students will be transferred to JNTUH for award of B. Tech. degree in the concerned B. Tech. specialization. Ex. B.Tech (ECE) for ECE students & B.Tech (CSE) for CSE students A separate certificate may be given to the students on the trained/earned course credits, if required.
4. The students have to pay the tuition fee to their respective colleges as per the norms.
5. No additional fee needs to be paid to either VEDA IIT / Consortium of Industries or JNTUH except for examination fee.
6. The students have to follow the academic regulations & attendance requirements of both JNTUH & VEDA IIT.
7. VEDA IIT has to send monthly attendance & internal examination marks to JNTUH.
8. The students have to attend the course classes at VEDA Educational Society (VEDA IIT), Aydiv IT Park, Hyderabad.
9. The parent colleges have to submit the undertaking for their interested students to permit to attend the classes at VEDA IIT.
10. JNTUH has to agree for transfer of credits earned at VEDA IIT to JNTUH for the award of UG degree.
11. Students once opted for this proposal, there is no exit policy in middle of this program, either in IV-I or IV-II and request to re-join in their parent colleges.

12. VEDA IIT has to provide the placements for all the trained & successfully completed students as per the terms and conditions of the companies.
13. As this proposal is sponsored by the Consortium of Industries in collaboration with VEDA IIT, the students are expected to submit, prior to joining the VEDA Program, a commitment agreement for a minimum period of 3 years. The clause for exit policy commitment agreement should also be well defined by the consortium at the time of admission.
14. The following table gives the proposed courses offered in B. Tech. - ECE/EEE/EIE/CSE IV Year I & II Semesters at VEDA IIT:

IV Year I Semester

S. No.	Course	Course Title	L	T	P	Credits
1.	PC	Advanced Logic Design with Functional Blocks & State Machine	3	1	0	4
2.	PE-III	Unix & Scripting Languages	3	0	0	3
3.	PE-IV	Choose one of the following: 1. VLSI Design with Verilog 2. X86 Architecture	3	0	0	3
4.	OE-II	Choose one of the following: 1. C++ & Verification Methodologies 2. Physical Design Basics 3. C++, Data Structures in C	3	0	0	3
5.	H&MS	Unix & Scripting Languages Laboratory	0	0	4	2
6.	PC	Choose one of the following Lab: 1. VLSI Verilog & System Verilog Laboratory 2. VLSI Physical Design Laboratory 3. C++, Data Structures in C Laboratory 4. X86 Laboratory	0	0	4	2
7.	PC	Project Stage-I	0	0	6	3
		Total Credits for PD/LD/ESD	**12**	**1**	**14**	**20**

IV Year II Semester

S. No.	Course	Course Title	L	T	P	Credits
1	PE-V	Choose one of the following: 1. VLSI Synthesis 2. Real Time Operating System	3	0	0	3
2	PE-VI	Choose one of the following: 1. System Verilog Assertions and UVM 2. Low Power Physical Design & Chip Finishing 3. Advanced Processor Architecture 4. Introduction to Web Development	3	0	0	3
3	OE-III	Choose one of the following: 1. Design for Testability (DFT) 2. ARM Architecture and Interface Protocols 3. Core JAVA 4. Full Stack	3	0	0	3
4	PC	Seminar	0	0	2	1
5	PC	Project Stage-II	0	0	20	10
		Total Credits for PD/LD/ESD	**9**	**0**	**22**	**20**

Hence, the Principals of University Constituent, Autonomous and Affiliated Colleges are requested to inform to the students and submit their Expression of Interest (EoI) indicating the list of students (with names & H.T Nos.) willing to opt. IV Year I & II semester courses in the area of VLSI & Embedded Systems offered at VEDA Educational Society (VEDA IIT), Aydiv IT Park, Hyderabad on or before 30.07.2022 to the Registrar, JNTUH and simultaneously register in www.vedaiit.org.

The entrance examination details & date will be intimate to the submitted list.

20/7/22

REGISTRAR

To
The Principals of the all University Constituent Colleges,
The Principals of the all Autonomous and Affiliated Colleges of JNTUH.